

RapidIO® 4.x BRC1 LP-Serial Endpoint Core Product Brief

Features

- Implements a complete RapidIO Endpoint solution.
- Compliant with Rev. 4.1 of the specification.
- Implements RapidIO Error Management Extensions.
- Supports 1x, 2x, and 4x link widths at BRC1 data rates.
- Supports the High Availability/Redundant System Hardware (HARSH) profiles
- Supports the MECS Time Synchronization Protocol.
- AXI4 interfaces for target, initiator, and messaging functions.
- Management Entity with integrated decoder for RapidIO maintenance transactions.
- IP-XACT support for rapid integration.
- Available for Xilinx and Intel FPGAs.
- Porting kit is available for ASIC targets.

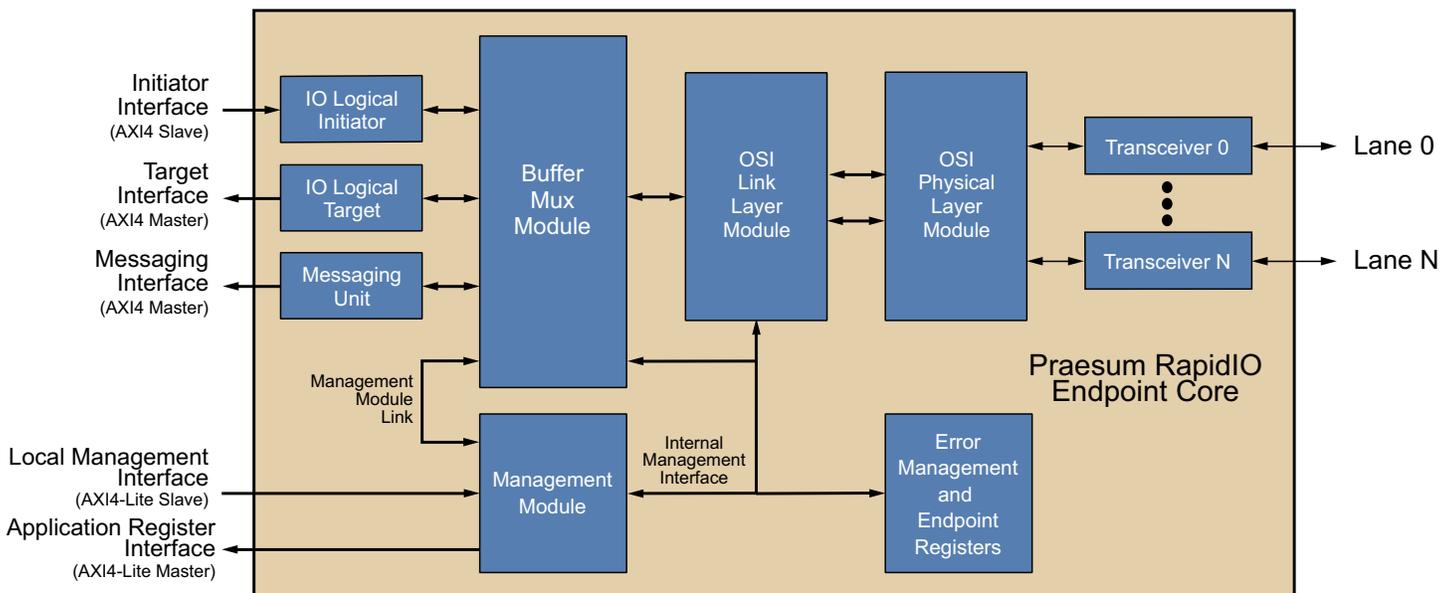
Description

The BRC1 LP-Serial Endpoint Core implements a complete RapidIO endpoint core capable of supporting link rates of up to 5.0 Gbps per lane. It includes shared memory and messaging logical layer functions. It also includes functions that allow the endpoint to be managed with or without a local processor. Figure 1 illustrates the overall architecture of the core.

The core integrates an IO Logical Layer Initiator block that maps AXI4 transactions into RapidIO IO Logical request packets. The IO Logical Layer Target block maps RapidIO IO Logical request packets into AXI4 transactions on the user interface. Together these functions support the transparent, low latency sharing of memory across the link.

The HARSH profile support provide a range of features that support the creation of high availability systems. This includes MECS timestamp synchronization that coordinates timing functions across the system with nano-second accuracy. The error management functions provide detailed traceability of system level errors along with optional error timestamping to assist with error analysis.

Figure 1 RapidIO® 4.x BRC1 LP-Serial Physical Layer Endpoint Core Block Diagram



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