RapidIO® 4.x BRC1 LP-Serial Endpoint Streaming Core Product Brief

Features

- Implements a complete RapidIO Endpoint solution for streaming data.

- Compliant with Rev. 4.1 of the specification.

- Implements RapidIO Error Management Extensions.

- Supports 1x, 2x, and 4x link widths at BRC1 data rates.

- Supports the High Availability/Redundant System Hardware (HARSH) profiles

- Supports the MECS Time Synchronization Protocol.

- AXI4-Stream interfaces for sensor data.

- Management Entity with integrated decoder for RapidIO maintenance transactions.

- IP-XACT support for rapid integration.

- Available for Xilinx and Intel FPGAs.

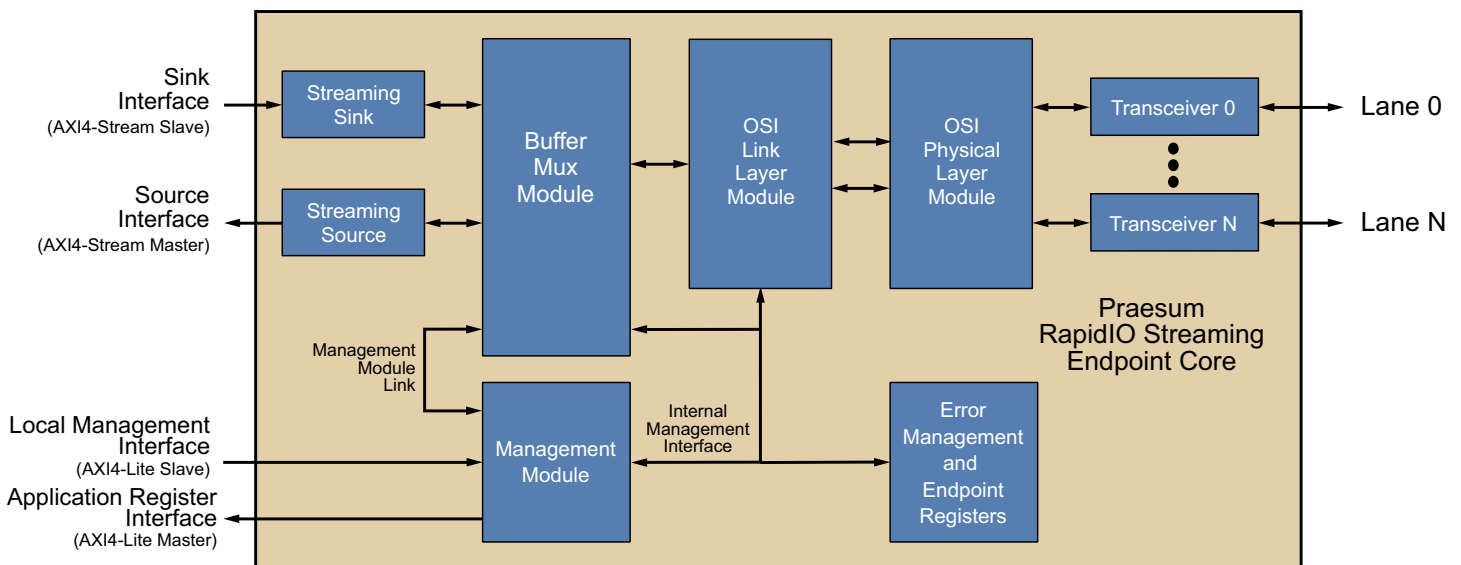- Porting kit is available for ASIC targets.

Description

The BRC1 LP-Serial Endpoint Streaming Core implements a complete RapidIO endpoint core capable of supporting link rates of up to 5.0 Gbps per lane. It includes functions that allow the endpoint to be managed with or without a local processor. Figure 1 illustrates the overall architecture of the core.

The core integrates a streaming sink block that maps AXI4-Stream transactions into RapidIO Type 9 request packets. The streaming source block maps RapidIO Type 9 request packets to AXI4-Stream transactions.

The HARSH profile support provide a range of features that support the creation of high availability systems. This includes MECS timestamp synchronization that coordinates timing functions across the system with nano-second accuracy. The error management functions provide detailed traceability of system level errors along with optional error timestamping to assist with error analysis.

Figure 1 RapidIO® 4.x BRC1 LP-Serial Physical Layer Streaming Endpoint Core Block Diagram