

Features

- Implements the complete RapidIO Physical Layer 1x/4x LP-Serial protocol.
- Compliant with Rev. 1.2 of the specification
- Implements Error Management Extensions
- 64-bit internal data paths.
- Hardware error recovery.
- Flexible SERDES interface supports industry standard multi-gigabit serial transceiver blocks.
- Flexible buffer management scheme suitable for end node and switch port implementation.

Description

The Physical Layer 1x/4x LP-Serial Core implements the OSI link layer and OSI physical layer functions that are defined in the RapidIO Physical Layer 1x/4x LP-Serial Specification Rev. 1.2. It has been partitioned so that to be used in both end-station and switch port applications.

Figure 1 illustrates the overall architecture of the implementation. The core consists of two modules, the OSI Link Layer Module (OLLM) and the OSI Physical Layer Module (OPLM). These modules break up the functionality of the RapidIO Physical Layer 1x/4x LP-Serial Specification into blocks that correspond to the Link Layer (Layer 2) and Physical Layer (Layer 1) of the OSI protocol model.

Figure 1 Physical Layer 1x/4x LP-Serial Core Block Diagram

