

Features

- Implements the complete RapidIO Physical Layer 8/16 LP-LVDS protocol.
- Compliant with Rev. 1.2 of the specification
- Implements Error Management Extensions
- 64-bit internal data paths for high throughput at lower clock rates.
- Supports throttle symbol flow control.
- Hardware error recovery.
- Flexible buffer management scheme suitable for end station and switch port applications.

Description

The Physical Layer 8/16 LP-LVDS Core implements the physical layer functions defined in the RapidIO Physical Layer 8/16 LP-LVDS Specification Rev. 1.2. It has been partitioned so that to be used in both end station and switch port applications.

Figure 1 illustrates the overall architecture of the core. It consists of two modules, the OSI Link Layer Module (OLLM) and the OSI Physical Layer Module (OPLM). These modules break up the functionality of the RapidIO Physical Layer 8/16 LP-LVDS Specification into blocks that correspond to the Link Layer (Layer 2) and Physical Layer (Layer 1) of the OSI protocol model.

Figure 1 Physical Layer 8/16 LP-LVDS Core Block Diagram

