

Features

- Motherboard form factor compatible with the ATX specification revision.
- One 3.3V, 32-bit PCI slot with a single 1x/4x LP-Serial RapidIO interface.
- One 5V, 32-bit PCI slot with a single 1x/4x LP-Serial RapidIO interface.
- One 3.3V, 32-bit PCI slot with a single 8/16 LP-LVDS RapidIO interface.
- One 5V, 32-bit PCI slot with a single 8/16 LP-LVDS RapidIO interface.
- Evaluation version of SwitchKit four-port RapidIO Switching IP

Description

The RapidIO Hardware Inter-operability Platform (HIP) motherboard is designed as a demonstration vehicle for Praesum's RapidIO Intellectual Property (IP) cores. It includes evaluation versions of the 8/16 LP-LVDS, and 1x/4x LP-Serial physical layer cores, as well as four port RapidIO switch.

Figure 1 illustrates the overall architecture of the board. A Xilinx Virtex-II Pro[™] FPGA hosts the IP cores, and includes debug and monitoring firmware running on the PowerPC processor.

Figure 1 RapidIO HIP Motherboard Block Diagram

